

VLSI Design

Lecture 5: Design Rules and Fabrication

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Adapted with modifications from lecture notes
prepared by author (from Prentice Hall PTR)

Topics

- Design rules and fabrication
- SCMOS scalable design rules
- Stick diagrams

Why we need design rules

- Masks are tooling for manufacturing.
- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Manufacturing problems

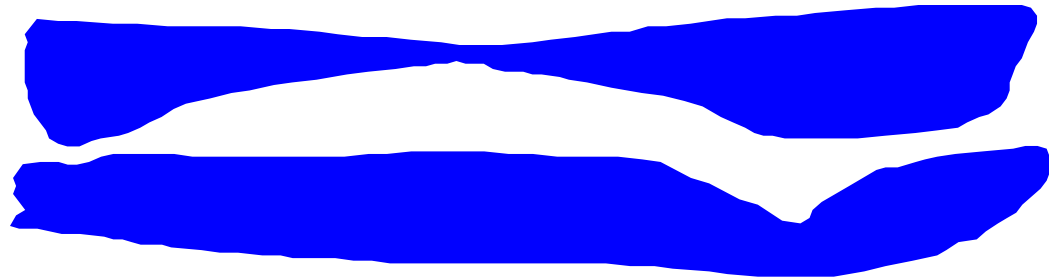
- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in temperature.
- Variations in oxide thickness.
- Impurities.
- Variations between lots.
- Variations across a wafer.

Transistor problems

- Variations in threshold voltage:
 - oxide thickness;
 - ion implantation;
 - poly variations.
- Changes in source/drain diffusion overlap.
- Variations in substrate.

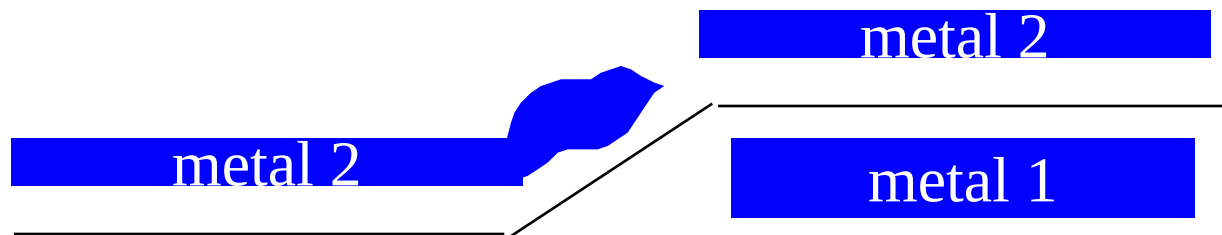
Wiring problems

- Diffusion: changes in doping → variations in resistance, capacitance.
- Poly, metal: variations in height, width → variations in resistance, capacitance.
- Shorts and opens:



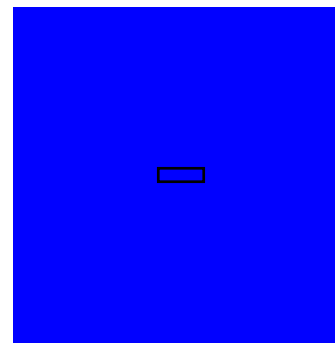
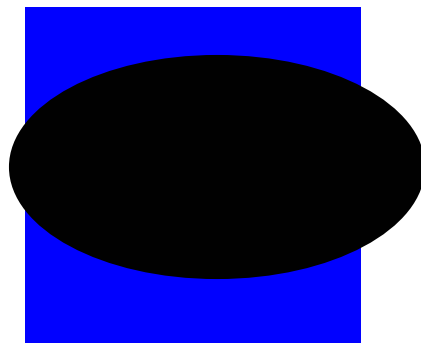
Oxide problems

- Variations in height.
- Lack of planarity → step coverage.



Via problems

- Via may not be cut all the way through.
- Undersize via has too much resistance.
- Via may be too large and create short.



MOSIS SCMOS design rules

1. Designed to scale across a wide range of technologies.
2. Designed to support multiple vendors.
3. Designed for educational use.
 - Therefore, fairly conservative.

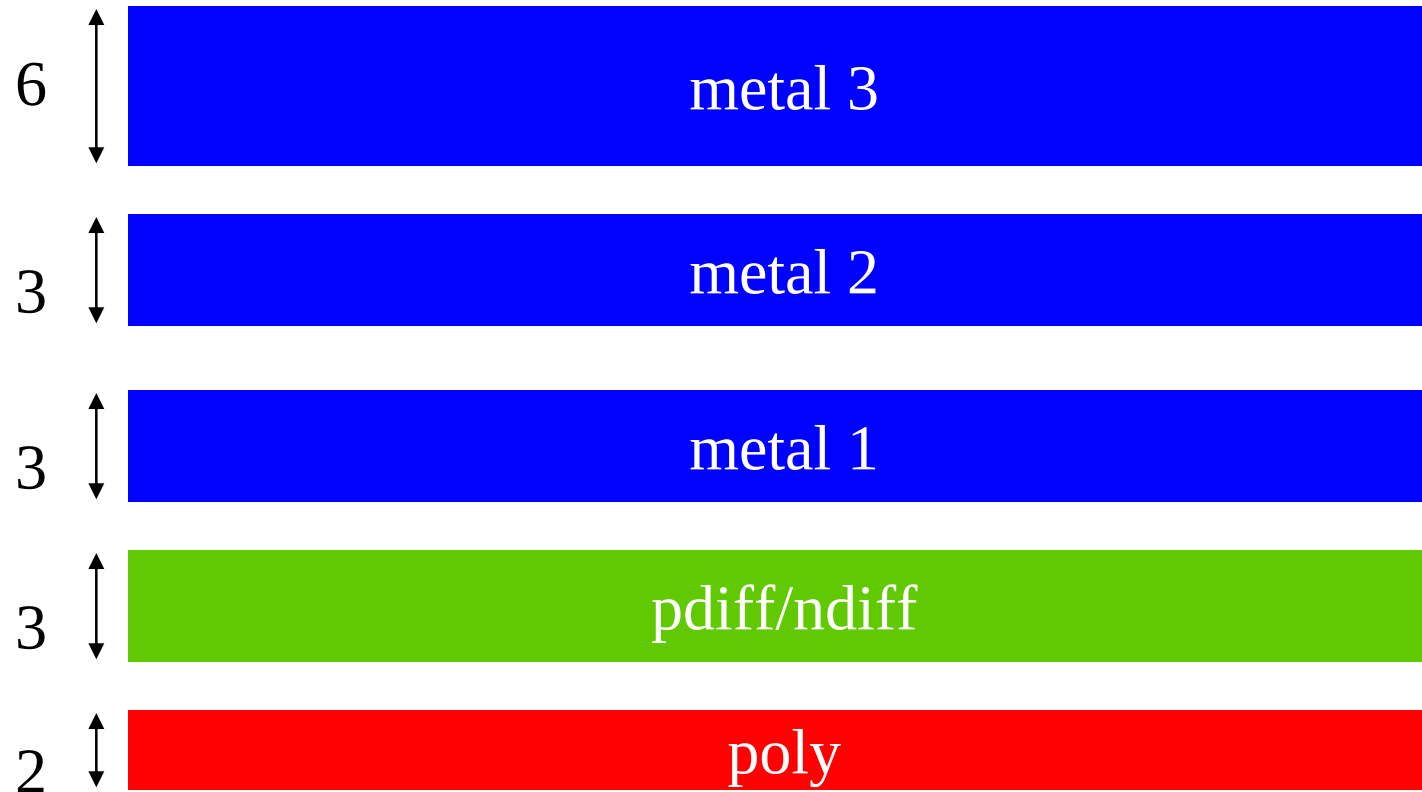
λ and design rules

- λ is the size of a minimum feature.
- Specifying λ particularizes the scalable rules.
- Parasitics are generally not specified in λ units.

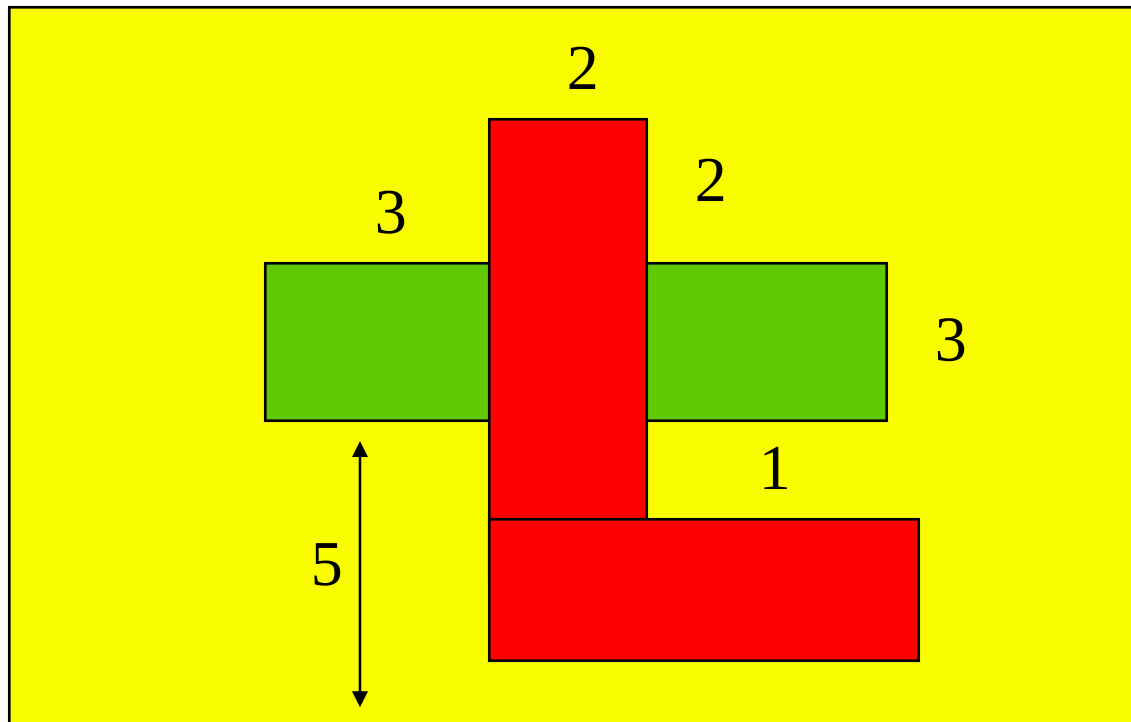
Scaling

- Scale all chip parameters by x :
 $W' \rightarrow W/x$, $L' \rightarrow L/x$, $V' \rightarrow V/x$, etc.
- Transistor current shrinks:
 - $I'/I = 1/x$.
- But capacitance shrinks more, so chip speeds up:
 - $(C'V'/I')/(CV/I) = 1/x$.
- Shrinking makes chip faster and smaller.

Wires

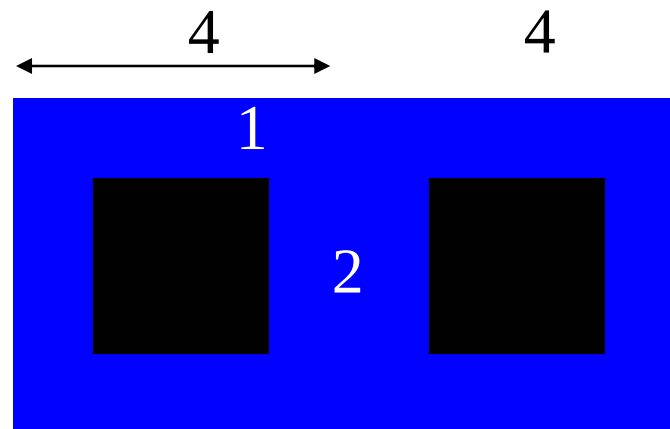


Transistors



Vias

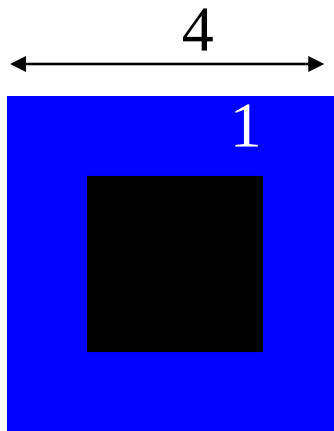
- Types of via: metal1/diff, metal1/poly, metal1/metal2.



Metal 3 via

- Type: metal3/metal2.
- Rules:
 - cut: 3 x 3
 - overlap by metal2: 1
 - minimum spacing: 3
 - minimum spacing to via1: 2

Tub tie



Spacings

- Diffusion/diffusion: 3
- Poly/poly: 2
- Poly/diffusion: 1
- Via/via: 2
- Metal1/metal1: 3
- Metal2/metal2: 4
- Metal3/metal3: 4

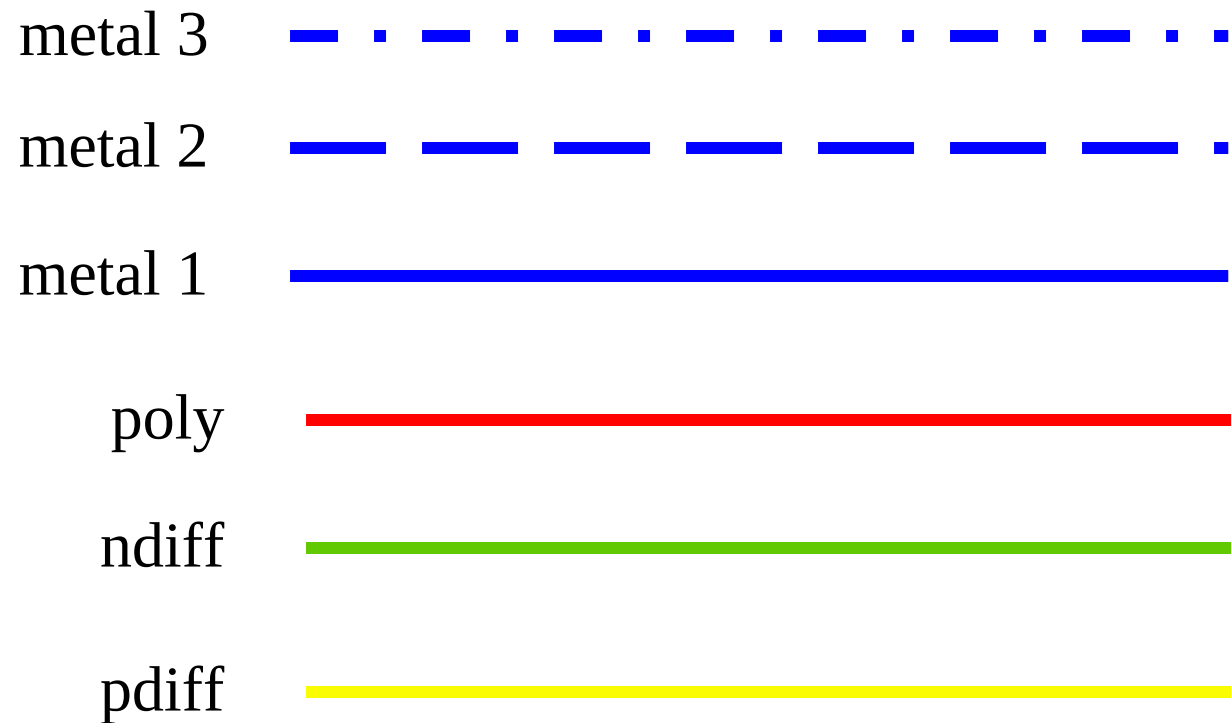
Overglass

- Cut in passivation layer.
- Minimum bonding pad: 100 μm
- Pad overlap of glass opening: 6
- Minimum pad spacing to unrelated metal2/3: 30
- Minimum pad spacing to unrelated metal1, poly, active: 15

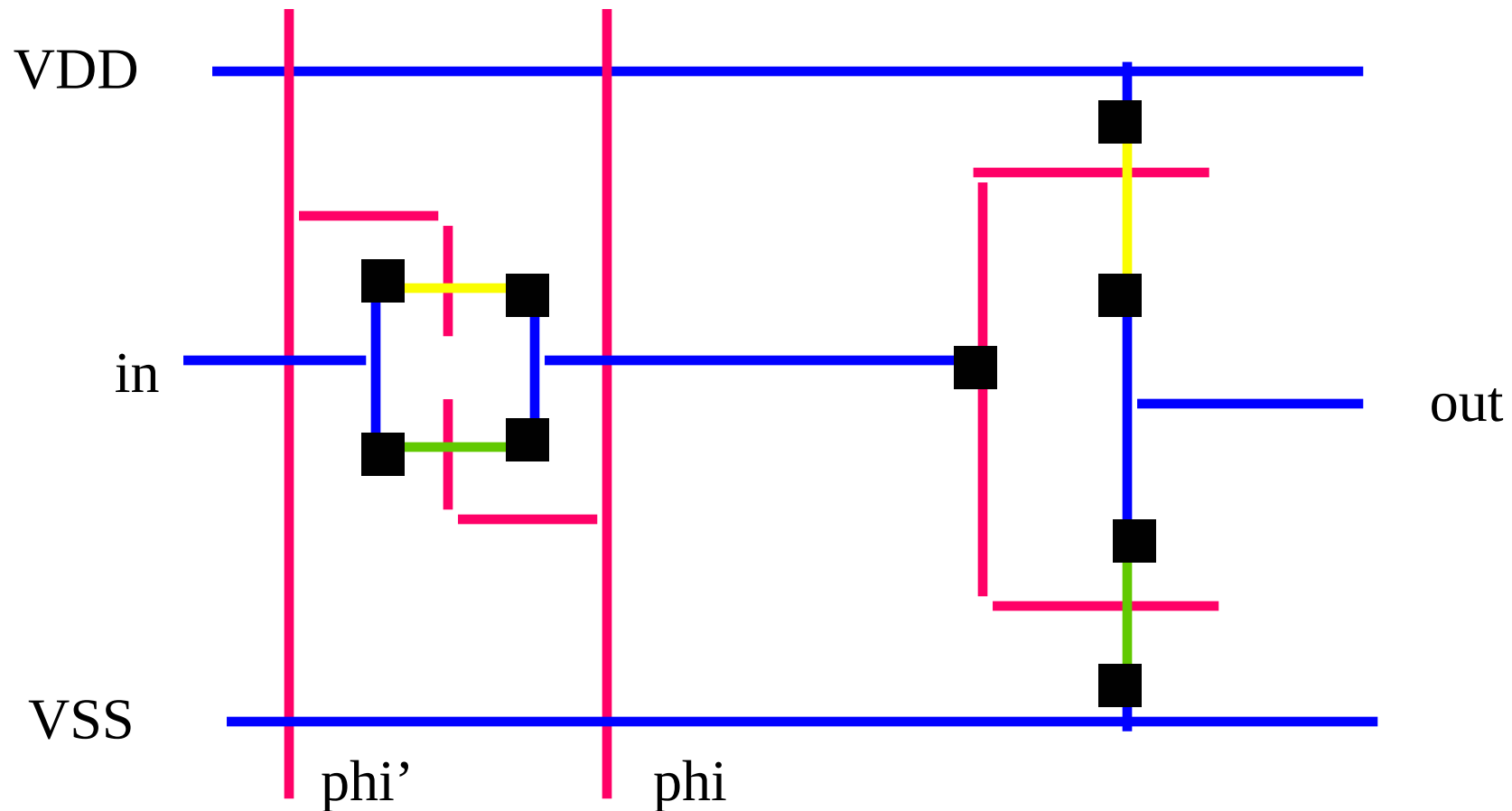
Stick diagrams

- A stick diagram is a cartoon of a layout.
- Does show all components/vias (except possibly tub ties), relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick layers

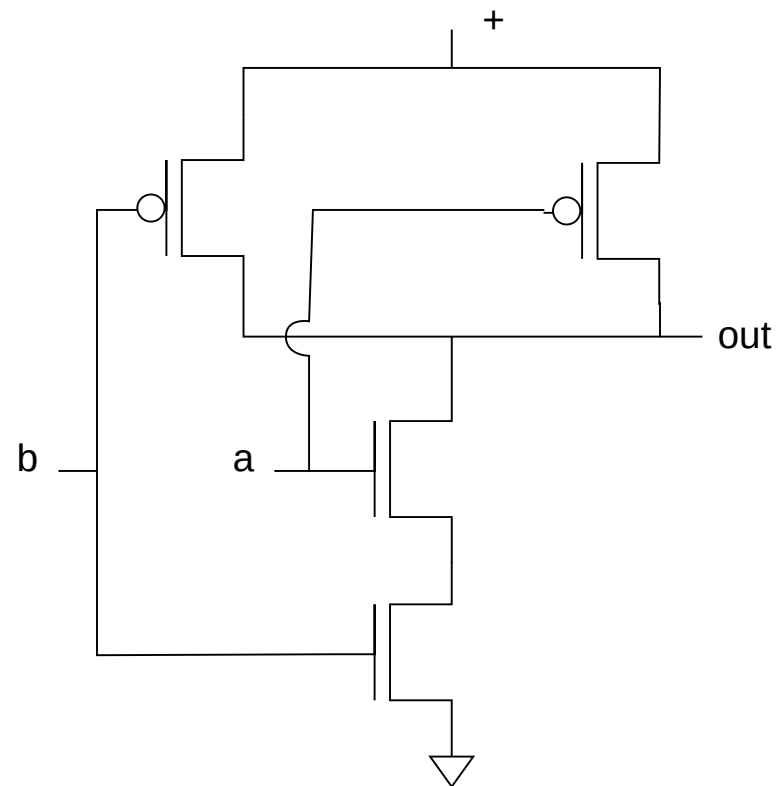


Dynamic latch stick diagram

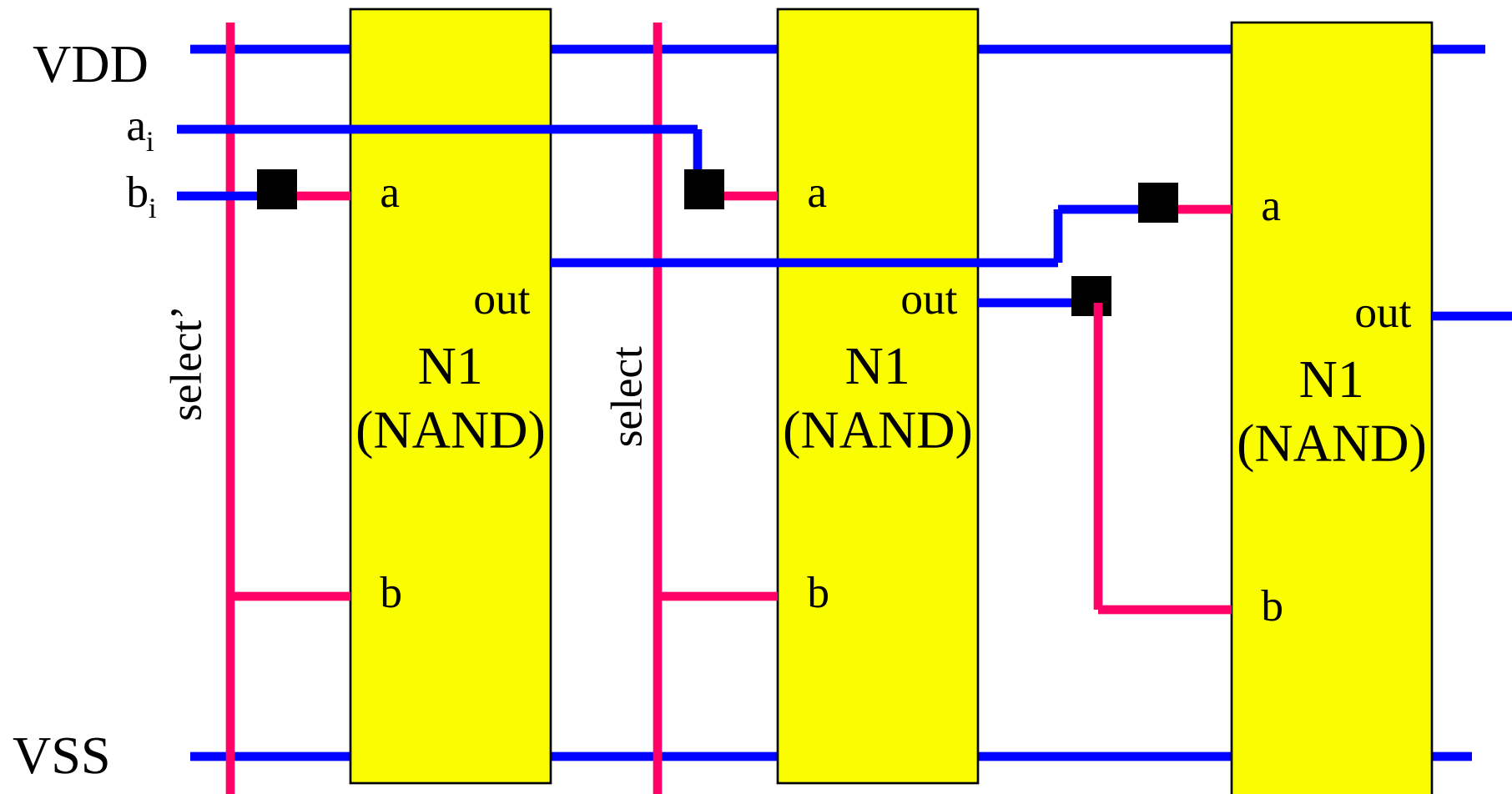


Sticks design of multiplexer

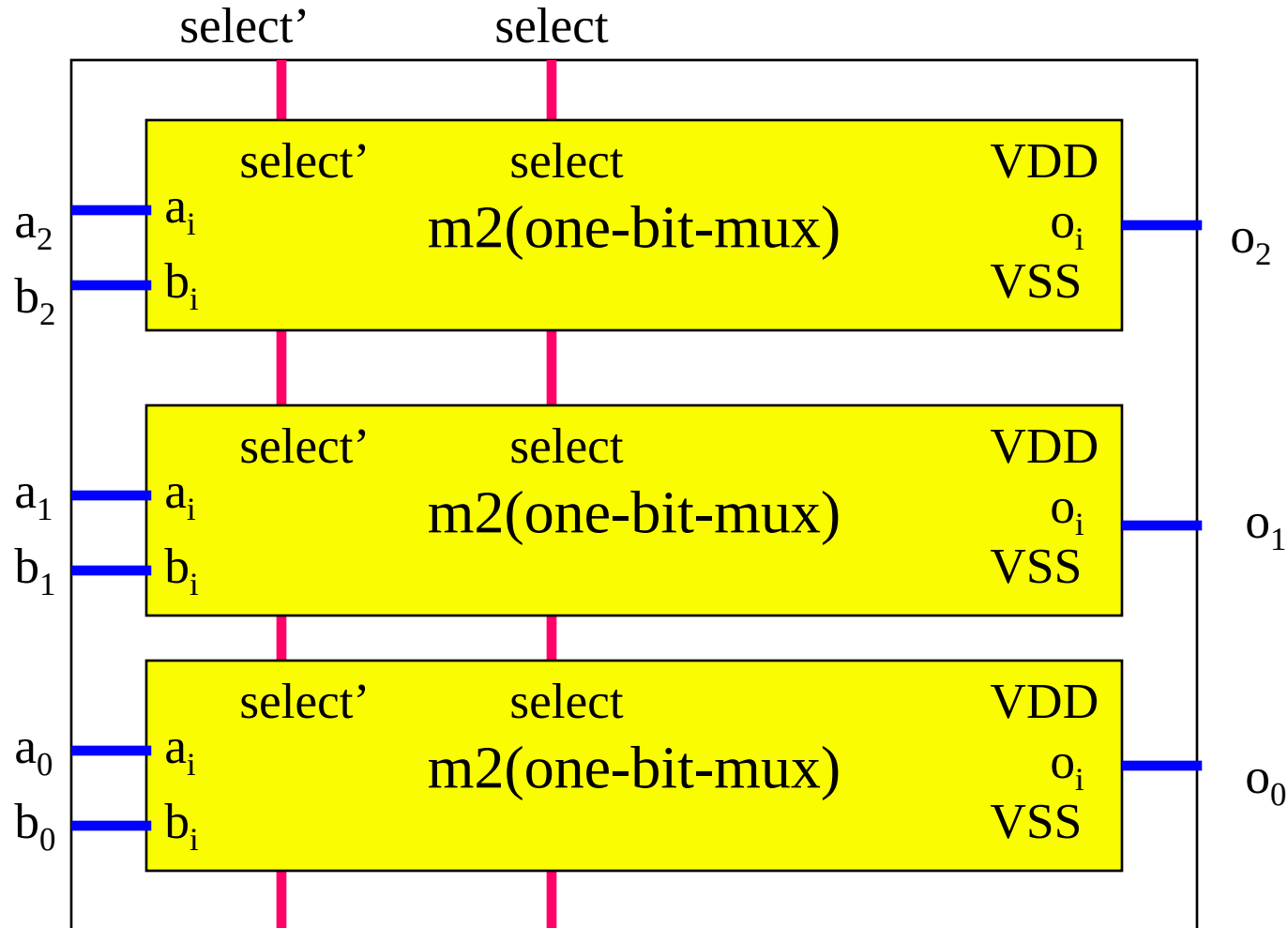
- Start with NAND gate:



One-bit mux sticks



3-bit mux sticks



Layout design and analysis tools

- Layout editors are interactive tools.
- Design rule checkers are generally batch--
-identify DRC errors on the layout.
- Circuit extractors extract the netlist from the layout.
- Connectivity verification systems (CVS) compare extracted and original netlists.

Automatic layout

- Cell generators (macrocell generators) create optimized layouts for ALUs, etc.
- Standard cell/sea-of-gates layout creates layout from pre-designed cells + custom routing.
 - Sea-of-gates allows routing over the cell.

Standard cell layout

